

## SEMICONDUCTOR DEVICE HAVING BURIED LAYER

### FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a semiconductor device and a method of fabricating the same and, more particularly, to a semiconductor device having a buried layer and a method of fabricating the same.

### BACKGROUND OF THE DISCLOSURE

[0002] Ultra-high voltage (ultra-HV) semiconductor devices are widely used in display devices, portable devices, and many other applications. Design goals of the ultra-HV semiconductor devices include high breakdown voltage, and low specific on-resistance. The specific on-resistance of the ultra-HV semiconductor device is limited by a doping concentration of a grade region of the device. When the doping concentration of the grade region decreases, the specific on-resistance increases.

### SUMMARY

[0003] According to an embodiment of the disclosure, a semiconductor device includes a substrate having a first conductivity type, a high-voltage well having a second conductivity type and formed in the substrate, a drift region formed in the high-voltage well, and a buried layer having the first conductivity type formed below the high-voltage well and vertically aligned with the drift region.

[0004] According to another embodiment of the disclosure, a method for fabricating a semiconductor device is provided. The method includes providing a substrate having a first conductivity type, forming a buried layer having the first conductivity type in the substrate, forming an epitaxial layer having the first conductivity type over the substrate formed with the buried layer, forming a high-voltage well having a second conductivity type in the epitaxial layer, and forming a drift region in the high-voltage well, the drift region being vertically aligned with the buried layer.

[0005] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate disclosed embodiments and, together with the description, serve to explain the disclosed embodiments.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 schematically illustrates a cross-sectional view of an ultra-high voltage semiconductor device, according to an embodiment.

[0007] FIGS. 2A-2N schematically illustrate a process of fabricating the device of FIG. 1, according to an illustrated embodiment.

[0008] FIG. 3 is a graph showing drain characteristics of the device of FIG. 1, and of a device constructed as a comparative example.

[0009] FIG. 4 is a graph showing the drain characteristics of the device of FIG. 1 and of the device constructed as the comparative example.

[0010] FIG. 5 schematically illustrates a cross-sectional view of a device, according to an illustrated embodiment.

[0011] FIG. 6 schematically illustrates a cross-sectional view of a device, according to an illustrated embodiment.

[0012] FIG. 7 schematically illustrates a cross-sectional view of a device, according to an illustrated embodiment.

[0013] FIG. 8 schematically illustrates a cross-sectional view of an insulated gate bipolar transistor, according to an illustrated embodiment.

[0014] FIG. 9 schematically illustrates a cross-sectional view of an ultra-HV diode, according to an illustrated embodiment.

### DETAILED DESCRIPTION

[0015] Reference will now be made in detail to the present embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0016] FIG. 1 schematically illustrates a cross-sectional view of an ultra-HV semiconductor device 10 (hereinafter referred to as “device 10”), according to an illustrated embodiment. Device 10 is an N-type lateral diffused metal oxide semiconductor (LDMOS) device that is designed to accommodate high-voltage operation (e.g., 40V or higher) or even ultra-high-voltage operation (e.g., 400V or higher) relatively to other semiconductor devices. As illustrated in FIG. 1, device 10 includes a P-type substrate (P-sub) 100, and a high-voltage N-well (HVNW) 120 formed in P-sub 100. A first P-well (PW) 125 is formed in HVNW 120 and functions as a source well. A second PW 126 is formed outside and adjacent to HVNW 120 and functions as a bulk well. A drift region 130 is formed in HVNW 120 and spaced apart from first PW 125. Drift region 130 includes a P-top region 135 and an N-grade region 140 formed above P-top region 135. An insulation layer 150 provided, for example, as a field oxide (FOX), is formed on P-sub 100. A gate oxide layer 160 is formed on a side (i.e., right-side) edge portion of first PW 125. A gate layer 165 is formed on gate oxide layer 160. Spacers 170 are formed on side walls of gate layer 165. A first N<sup>+</sup>-region 175 is formed in HVNW 120 and constitutes a drain region of device 10. A second N<sup>+</sup>-region 176 is formed in first PW 125 adjacent to a side (e.g., left-side) edge portion of gate layer 165. A first P<sup>+</sup>-region 180 is formed in first PW 125 adjacent to second N<sup>+</sup>-region 176. Second N<sup>+</sup>-region 176 and first P<sup>+</sup>-region 180 together constitute a source region of device 10. A second P<sup>+</sup>-region 181 is formed in second PW 126 and constitutes a bulk region of device 10. An interlayer dielectric (ILD) layer 190 is formed on P-sub 100. A contact layer 195 provided, for example, as a metal layer (M1), is formed on ILD layer 190. Contact layer 195 includes a plurality of isolated contact portions for conductively contacting different portions of the structures formed in P-sub 100 via different openings formed in ILD layer 190. Specifically, contact layer 195 includes a first contact portion 196 that conductively contacts first N<sup>+</sup>-region 175, a second contact portion 197 that conductively contacts gate layer 165, a third contact portion 198 that conductively contacts second N<sup>+</sup>-region 176 and first P<sup>+</sup>-region 180, and a fourth contact portion 199 that conductively contacts second P<sup>+</sup>-region 181. Additional ILD layers and contact layers can be formed on P-sub 100.

[0017] Device 10 also includes a pre-HVNW 105 and a P-type buried layer (PBL) 110 formed below HVNW 120, i.e., between a bottom of HVNW 120 and P-sub 100. Specifically, pre-HVNW 105 is formed under and adjacent to a bottom surface of HVNW 120. PBL 110 is disposed above pre-HVNW. Pre-HVNW 105 and PBL 110 are vertically (i.e., along a thickness direction of P-sub 100) aligned with and substantially overlap drift region 130.